

PFO012

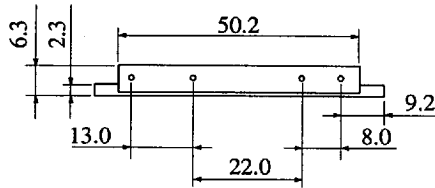
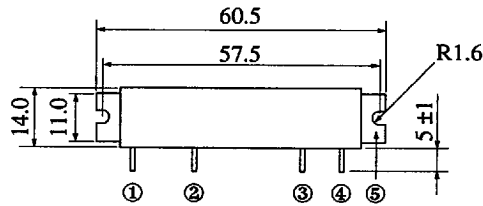
HITACHI/(OPTOELECTRONICS)

HIGH FREQUENCY POWER MOS FET MODULE

UHF Band 872-905 MHz

■ FEATURES

- Include Input and Output Matching Circuit
- Easy to Control Output Power
- Superior to Stability at Load Mismatching



- ① Pin
 - ② V_{APC}
 - ③ V_{DD}
 - ④ Pout
 - ⑤ CND
- (Dimensions in mm)

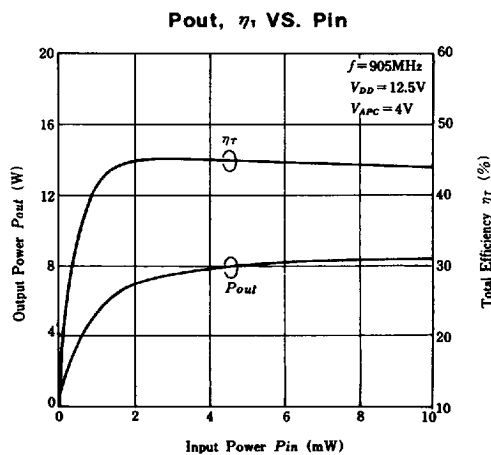
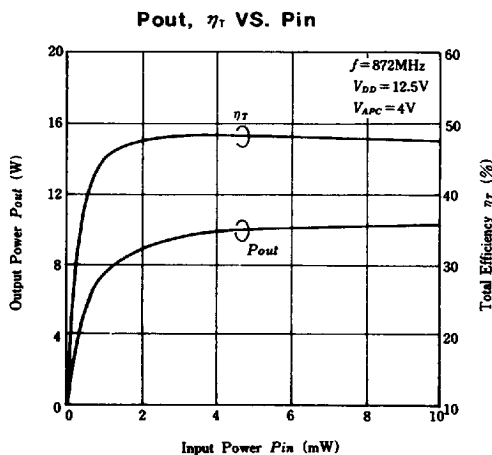
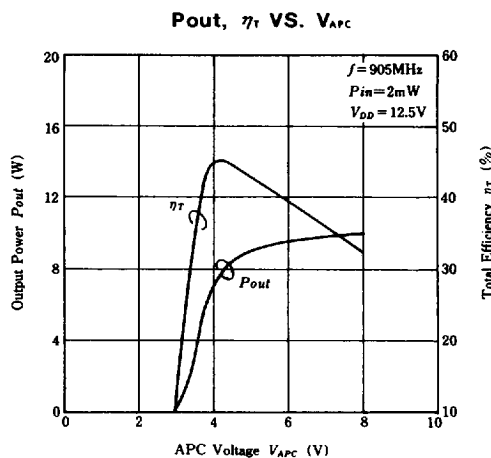
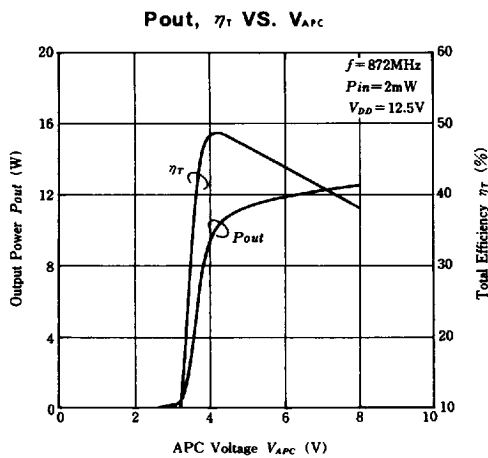
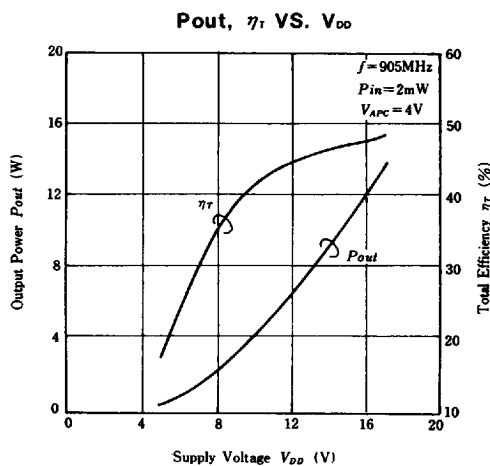
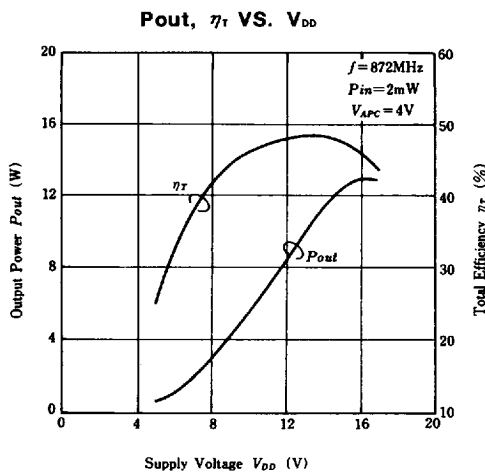
■ ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

| Item | Symbol | Rating | Unit |
|------------------------------------|-------------|----------|------------------|
| Supply Voltage | V_{DD} | 17 | V |
| Maximum Circuit Current | I_D | 3.0 | A |
| APC Voltage | V_{APC} | 8 | V |
| Maximum Input Power | P_{in} | 20 | mW |
| Operating Maximum Case Temperature | $T_{c(op)}$ | -40~+100 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -45~+125 | $^\circ\text{C}$ |

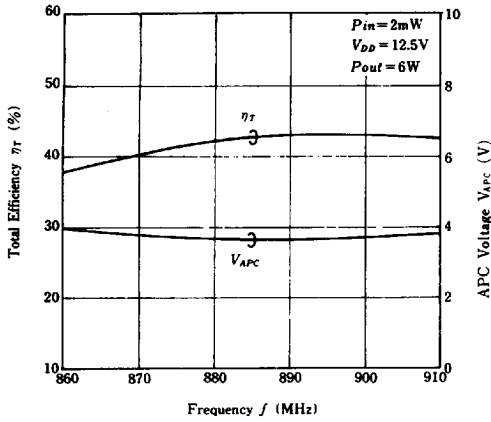
■ ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$)

| Item | Symbol | Test Condition | min. | typ. | max. | Unit |
|-------------------------|-----------|--|-------------------------|------|------|---------------|
| Drain Cutoff Current | I_{DS} | $V_{DD1} = V_{DD2} = 17\text{V}$, $V_{APC} = 0$ | — | — | 500 | μA |
| Total Efficiency | η_T | $f = 872, 905\text{MHz}$ | 35 | 40 | — | % |
| 2nd Harmonic Distortion | 2nd H.D. | $P_{in} = 2\text{mW}$ | — | -50 | -30 | dB |
| 3rd Harmonic Distortion | 3rd H.D. | $V_{DD} = 12.5\text{V}$ | — | -50 | -30 | dB |
| Input VSWR | VSWR(in) | $P_{in} = 6\text{W}$ (at APC Control) | — | 1.5 | 3.0 | — |
| Output VSWR | VSWR(out) | $Z_{in} = Z_{out} = 50\Omega$ | — | 1.5 | — | — |
| Stability | — | $V_{DD} = 12.5\text{V}$, $P_{in} = 2\text{mW}$, $f = 872\text{MHz}$, $P_{out} = 6\text{W}$ (at APC Control), $R_L = 50\Omega$, Output VSWR $\neq \infty$ All Phase, $t = 20\text{sec}$ | No Parastic Oscillation | | | — |

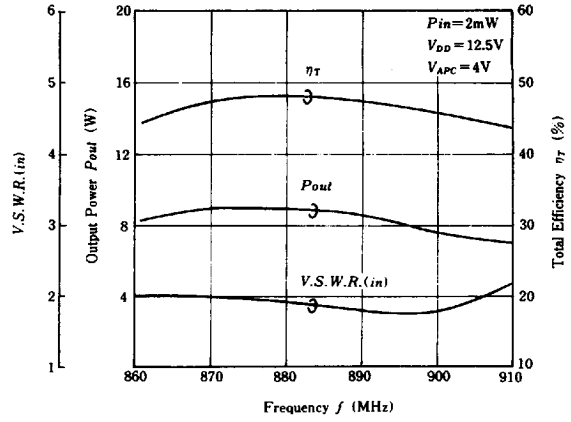
HITACHI/(OPTOELECTRONICS)



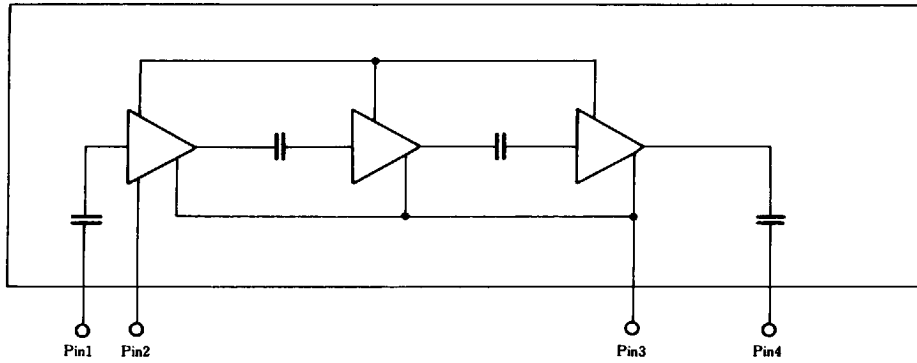
η_T , V_{APC} VS. FREQUENCY



η_T , P_{out} , VSWR VS. FREQUENCY



INTERNAL DIAGRAM



TEST SYSTEM DIAGRAM

